1. The simplest equation which implements the K-map shown below is:

		$\bar{C}$	C
$\bar{A}$	$\bar{B}$	0	0
$\bar{A}$	B	1	1
A	B	1	1
A	$\bar{B}$	0	1

A. $X = AC + B$ B. $X = A\bar{B}$ C. $AB\bar{C} + ABC + A\bar{B}C$ D. $AB + \bar{A}B$

Ans: A

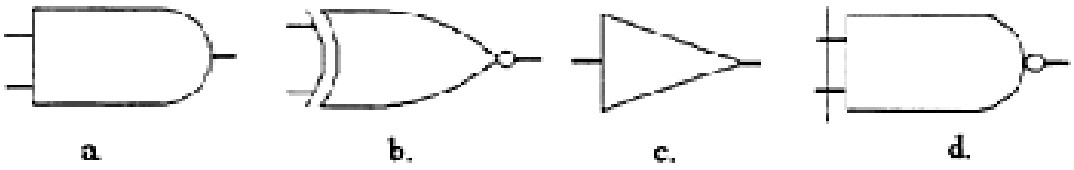
2. Convert BCD 0001 0010 0110 to binary.

A.1111110 B.1111101 C.1111000 D.1111111

3. How many 3-line-to-8-line decoders are required for a 1-of-32 decoder?

A. 1 B .2 **C. 4** D. 8

4. Which of the figures shown below represents the exclusive-NOR gate?



A. a **B b** C. c D. d

5. Which of the following statements accurately represents the two BEST methods of logic circuit simplification?

A. Boolean algebra and Karnaugh mapping

B. Karnaugh mapping and circuit waveform analysis

C. Actual circuit trial and error evaluation and waveform analysis

D. Boolean algebra and actual circuit trial and error evaluation

6. Which of the following combinations cannot be combined into K-map groups?

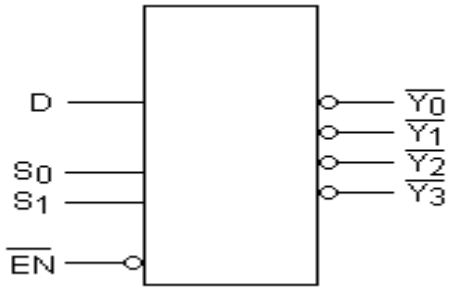
A. Corners in the same row B. Corners in the same column

C .Diagonal corners D. Overlapping combinations

7. Which gate is best used as a basic comparator?

A. NOR B. OR **C. Exclusive-OR** D. AND

8. The device shown here is most likely a _____.



A. comparator B. multiplexer **C. demultiplexer** D. parity generator

9. Each "1" entry in a K-map square represents:

A. a HIGH for each input truth table condition that produces a HIGH output.

B. a HIGH output on the truth table for all LOW input combinations.

C. a LOW output for all possible HIGH input conditions.

D. a DON'T CARE condition for all possible input truth table combination

10. Looping on a K-map always results in the elimination of:

A. variables within the loop that appear only in their complemented form.

B. variables that remain unchanged within the loop.

C. variables within the loop that appear in both complemented and uncomplemented form.

D. variables within the loop that appear only in their uncomplemented form

11. How many 4-bit parallel adders would be required to add two binary numbers each representing decimal numbers up through 30010?

A. 1 B. 2 **C. 3** D. 4

12. Which statement below best describes a Karnaugh map?A.

A. Karnaugh map can be used to replace Boolean rules.

B.The Karnaugh map eliminates the need for using NAND and NOR gates.

C.Variable complements can be eliminated by using Karnaugh maps.

D.Karnaugh maps provide a visual approach to simplifying Boolean expressions.

13. Which of the K-maps given below represents the expression X = AC + BC + B?

		$\bar{C}$	C
$\bar{A}$	$\bar{B}$	1	1
$\bar{A}$	B	1	1
A	B	0	0
A	$\bar{B}$	0	0

a.

		$\bar{C}$	C
$\bar{A}$	$\bar{B}$	0	1
$\bar{A}$	B	0	0
A	B	1	1
A	$\bar{B}$	1	1

b.

		$\bar{C}$	C
$\bar{A}$	$\bar{B}$	0	0
$\bar{A}$	B	1	1
A	B	1	1
A	$\bar{B}$	0	1

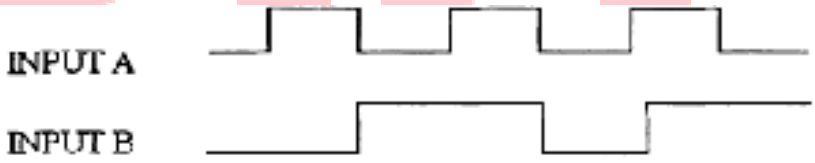
c.

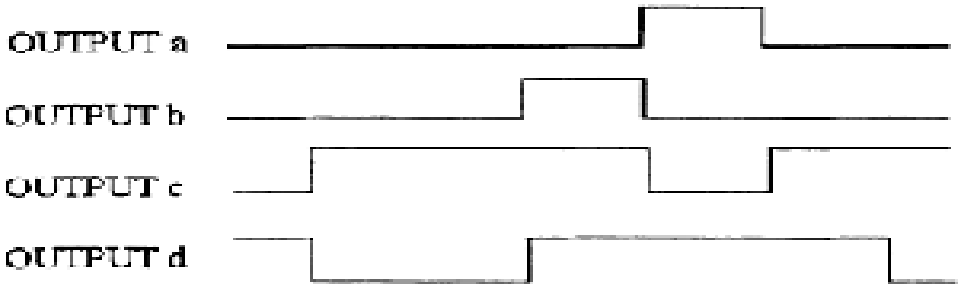
		$\bar{C}$	C
$\bar{A}$	$\bar{B}$	1	1
$\bar{A}$	B	0	1
A	B	0	1
A	$\bar{B}$	1	1

d.

Ans: C

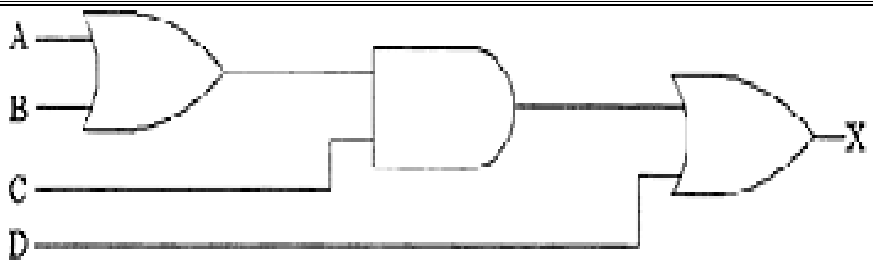
14. For a two-input XNOR gate, with the input waveforms as shown below, which output waveform is correct?





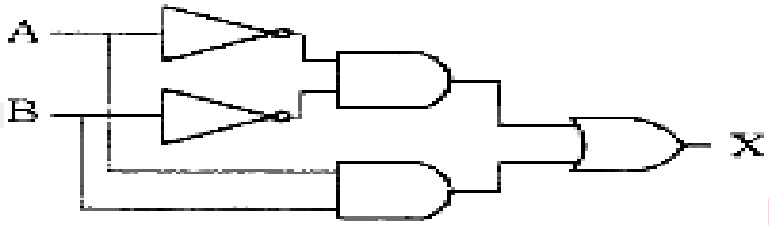
Ans: D

15. Solve the network in the figure given below for X.



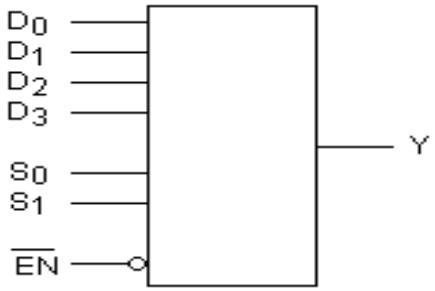
A. A + BC + D **B. ((A + B)C) + D** C. D(A + B + C) D. (AC + BC)D

16. What type of logic circuit is represented by the figure shown below?



A.XOR **B.XNOR** C.XAND D.XNAND

17. The device shown here is most likely a _____.



A.comparator **B.multiplexer** C.demultiplexer D.parity generator

18. When adding an even parity bit to the code 110010, the result is _____.

A.1110010 B.1111001 C.110010 D.001101

18. Convert the binary number 0000.1010 to decimal.

A) 0.10 B) 0.55 C) 0.50 **D) 0.625**

19. What is the decimal value of 2^{-2} ?

A) 0.5 B) 0.125 C) 0.2 **D) 0.25**

20. The hexadecimal equivalent of a binary 0010111101111110 is _____.

A)$2F77_{16}$ B) $4EEE_{16}$ C) $77F2_{16}$ **D) $2F7E_{16}$**

21. Convert decimal 31 to octal.

A) 37_8 B) 43_8 C) 33_8 D) 30_8

22.The decimal equivalent of the BCD value 0011 1001 0010 is _____.

A) 490_{10} **B) 392_{10}** C) 982_{10} D) 413_{10}

23) What is the decimal value of 2^{-1}?

A) 0.1 B) 0.25 **C) 0.5** D) 0.05

24) The hexadecimal equivalent of a binary 10000111 is _____.

A) 93_{16} B) 81_{16} **C) 87_{16}** D) 77_{16}

25) The hexadecimal equivalent of a binary 10100101 is _____.

A) $A4_{16}$ **B) $A5_{16}$** C) $C3_{16}$ D) $B5_{16}$

26) The hexadecimal equivalent of a binary 10001100 is _____.

A) $8C_{16}$ B) $C8_{16}$ C) 86_{16} D) CC_{16}

27) Convert the binary number 1010.1100 to decimal.

A) 12.65 B) 10.875 C) 10.55 **D) 10.75**

28) The decimal equivalent of hexadecimal 102 is _____

A) 59_{10} **B) 258_{10}** C) 256_{10} D) 60_{10}

29) The binary equivalent of hexadecimal F2 is _____.

A) 11110010 B) 11100011 C) 11111100 D) 10100001

30) The BCD equivalent of decimal 88 is _____.

A) 1000 1000BCD B) 1010 1000BCD C) 1100 0010BCD D) 1001 0000BCD

31) The decimal equivalent of binary 0010111 is _____.

A) 48_{10} B) 22_{10} C) 19_{10} **D) 23_{10}**

32) Edge-triggered flip-flops must have:

A.very fast response times. B.at least two inputs to handle rising and falling edges.

C.a pulse transition detector. D.active-LOW inputs and complemented outputs

33. As a general rule for stable flip-flop triggering, the clock pulse rise and fall times must be:

A.very long. **B.very short.**

C. at a maximum value to enable the input control signals to stabilize.

D.of no consequence as long as the levels are within the determinate range of value.

34. The circuit that is primarily responsible for certain flip-flops to be designated as edge-triggered is the:

A.edge-detection circuit. B.NOR latch.
C.NAND latch. D.pulse-steering circuit.

35. Which statement BEST describes the operation of a negative-edge-triggered D flip-flop?

A.The logic level at the D input is transferred to Q on NGT of CLK.

B.The Q output is ALWAYS identical to the CLK input if the D input is HIGH.

C.The Q output is ALWAYS identical to the D input when CLK = PGT.

D.The Q output is ALWAYS identical to the D input.

36. Parity generation and checking is used to detect _____.

A. which of two numbers is greater B.**errors in binary data transmission**

C.errors in arithmetic in computers D.when a binary counter counts incorrectly

37. The AND-OR-INVERT gates are designed to simplify implementation of _____.

A.POS logic **B.DeMorgan's theorem**
C.NAND logic **D.**SOP logic

38. Occasionally, a particular logic expression will be of no consequence in the operation of a circuit, such as in a BCD-to-decimal converter. These result in _____ terms in the K-map and can be treated as either _____ or _____, in order to _____ the resulting term.

A. **don't care, 1's, 0's, simplify** B.spurious, AND's, OR's, eliminate

C. duplicate, 1's, 0's, verify D. spurious, 1's, 0's, simplify

39. A Karnaugh map will _____.

A.eliminate the need for tedious Boolean simplifications
B.allow any circuit to be implemented with just AND and OR gates
C.produce the simplest sum-of-products expression
D.give an overall picture of how the signals flow through the logic circuit

40. Parity generators and checkers use _____ gates.

A.exclusive-AND **B.exclusive-OR/NOR**
C.exclusive-OR **D.**exclusive-NAND

41. The _____ circuit produces a HIGH output whenever the two inputs are equal.

A.exclusive-AND **B.**exclusive-NAND
C.exclusive-NOR **D.**exclusive-OR

42. When Karnaugh mapping, we must be sure to use the _____ number of loops.

A.maximum B.**minimum** C.median D. Karnaugh

43. One reason for using the sum-of-products form is that it can be implemented using all _____ gates without much difficulty.

A.NOR **B.NAND** **C.**AND **D.**DOOR

44. The column weight of the "1" in the hexadecimal number 1AB is _____.

A.64 **B.256** **C.**512 **D.**1024

45. Which of the following is an important feature of the sum-of-products form of expressions?

A.All logic circuits are reduced to nothing more than simple AND and OR operations.

B.The delay times are greatly reduced over other forms.

C.No signal must pass through more than two gates, not including inverters.

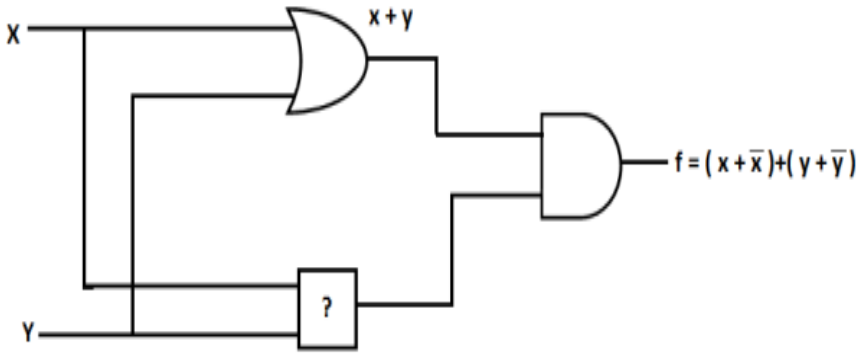
D.The maximum number of gates that any signal must pass through is reduced by a factor of two.

46. Which of the following can be represented for decoder?

a) Sequential circuit **b) Combinational circuit**

c) Logical circuit d) None of the mentioned

47. To make the following circuit a tautology ? marked box should be



A. OR gate B.AND gate C.**NAND gate** D.EX-OR GATE

48. BCD to seven segment conversion is a _____

a) Decoding process b) Encoding process

c) Comparing process d) None of the mentioned

49. Decoder is constructed from _____

a) Inverters b) AND gates

c) Inverters and AND gates d) None of the mentioned

50. A device which converts BCD into octal is called

A. encoder B. **decoder** **C.** code converter D. demultiplexer

51. $(11011)_2$ in BCD 8421 code is

A. **00011011** B. 00100111 **C.** 11011001 D. 01101100

52. $(1D)_{16}$ in BCD 8421 code is

A. **00011101** B. 00101001 **C.** 00011111 D. 00100100

53. The NAND gate can function as a NOT gate if

A. all inputs are connected together
B. inputs are left open
C. one input is set to 0
D. **one input is set to 1**

54. The NOR gate can function as a NOT gate if

A. all inputs are connected together
B. inputs are left open
C. one input is set to 0
D. one input is set to 1

55. An X-OR gate gives a high output

A. **if there are odd number of 1s**
B. if it has even number of 0s
C. if the decimal value of digital word is even
D. for odd decimal value

56. An exclusive NOR gate is logically equivalent to

A. inverter followed by an X-OR gate
B. **X-OR gate followed by an inverter**
C. NOT gate followed by a NOR gate
D complement of a NOR gate

57. The logic expression AB can be implemented by giving the inputs A and B to a two-input

A. NOR gate B. **NAND gate** **C.** X-OR gate D . X-NOR gate

58. The logic expression A + B can be implemented by giving inputs A and B to a two-input

A. NOR gate B. NAND gate **C.** X-OR gate D . X-NOR gate

59. NOT gates are to be added to the inputs of which gate to convert it to a NOR gate?

A. OR B. **AND** **C.** NAND D . X-NOR

60. The output of a NOR gate is high

A. **only when all the inputs are low**
B. only when all the inputs are high
C. only when at least one input is high
D . only when at least one input is low

61. System Transport Signal (STS) multiplexer multiplexes signals from multiple sources and creates

A. Optical Network
B. Optical Signal
B. Optical device
D. None of the Above

62. In STS Multiplexer, type of signal at input and output of an add/drop multiplexer is

A. Different B. Zero C.Converted **D.Same**

63. **The function of a multiplexer is**

A.to decode information
B.to select 1 out of N input data sources and to transmit it to single channel
C.to transit data on N lines
D.to perform serial to parallel conversion

64. **A combinational logic circuit which generates a particular binary word or number is**

A. **Decoder** B.Multiplexer C.Encoder D.Demultiplexer

65 **Which of the following circuit can be used as parallel to serial converter ?**

A. **Multiplexer** B. Demultiplexer C. Decoder D. Digital counter